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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **DEFENDANTS' RESPONSE BRIEF TO PLAINTIFFS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER** Date: November 30, 2012 Judge: Hon. Paul S. Grewal

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 JW
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 JW

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'336 patent	United States Patent No. 5,809,336
'749 patent	United States Patent No. 5,440,749
Otteson Decl.	Declaration of James C. Otteson in Support of Defendants' Responsive Brief to Plaintiff's Motion for Reconsideration of Certain Aspects of First Claim Construction Order
Chen Decl.	Declaration of Kyle D. Chen in Support of Motion for Reconsideration of Certain Aspects of First Claim Construction Order

Introduction

Declaratory judgment defendants TPL, Patriot and Alliacense (collectively "TPL") respectfully ask the Court to reaffirm Judge Ware's constructions of the terms "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" as found in claim 1 of U.S. Pat. No. 5,440,749 ("the '749 patent") and "clocking said central processing unit" as found in each claim of U.S. Pat. No. 5,809,336 ("the '336 patent"). As set forth in the Court's First Claim Construction Order ("FCCO"), the prosecution history for the reexamination of the '749 patent does not provide a basis for narrowing the claims as proposed by Plaintiffs during claim construction and, now, in their Motion for Reconsideration [Dkt. 358] ("Plaintiffs' Mtn."). Similarly, Judge Ware found the prosecution history of the '336 patent likewise fails to provide a basis for narrowing the claims as proposed by Plaintiffs. Judge Ware's constructions of these straightforward terms are consistent with the patent specifications, the plain and ordinary meanings of the terms themselves and the prosecution histories. Plaintiffs' Motion, moreover, raises *no new arguments* that have not been thoroughly considered by Judge Ware or, previously, by Judge Ward in the prior Texas litigation. Accordingly, TPL requests the Court deny Plaintiffs Mtn. and thereby construe the terms at issue therein consistent with the prior constructions set forth by Judge Ware.

Factual Background

A. The Patented Technology.

The two Asserted Patents at issue in Plaintiffs' Motion to Reconsider – U.S. Patent Nos. 5,440,749 and 5,809,336 – share the same specification, with slight differences in pagination. The '749 and '336 patents, together with related counterparts, have been the subject of at least 15 *ex parte* reexamination challenges before the U.S. Patent and Trademark Office ("PTO"). The first '336 patent reexamination certificate issued on December 15, 2009; the second reexamination certificate issued on November 3, 2010. Collectively, the '336 patent has withstood 607 prior art references that were cited in reexamination, including Judge Ward's claim construction order from the earlier Texas litigation, and the associated briefing and evidence. *See* Otteson Decl., Exh. A

('336 Patent and Re-exam Certificate). Similarly, the PTO recently issued reexamination certificates for the '749 patent over 846 cited references. *See* Otteson Decl., Exh. B ('749 patent and Re-exam Certificate). To say that the claims of the '749 and '336 patents have been closely scrutinized by the PTO would be an understatement.

B. The '336 Patent.

Microprocessors are complex machines with millions of individual parts whose operation requires coordination – both internally and with external components – for the chip to function properly. This coordination is performed by clock signals. The '336 patent, entitled "High Performance Microprocessor Having Variable Speed System Clock," teaches the use of two independent clocks in a microprocessor system: (1) an on-chip first clock to time the CPU; and (2) a second independent clock to time the input/output (I/O) interface. This innovation was widely adopted by the industry and became fundamental to the increased speed and efficiency of modern microprocessors. Decoupling the system clock from the I/O clock allowed the clocks to run independently (or "asynchronously"), freeing the system clock – and thus the CPU – to run faster when needed or, more slowly when not needed to conserve power.

C. The '749 Patent.

Microprocessor instructions are usually stored in a memory that is slower than the CPU. The '749 patent, entitled "High Performance, Low Cost Microprocessor Architecture," teaches a processor that fetches multiple instructions at a time, and then supplies them to the CPU's instruction register in parallel (at the same time) during the same memory cycle they are fetched. Since memory is generally slower than the CPU, being able to fetch and supply more than one instruction at a time increases the amount of instructions the CPU can receive in a given time, and thus increases instruction bandwidth.

Argument

I. THE LEGAL STANDARDS APPLICABLE TO CLAIM CONSTRUCTION.

This Court is well-versed in the general principles applicable to claim construction. *Sealant Sys. Int'l, Inc. v. TEK Global S.R.L.*, Nos. 11–CV–00774–PSG, 11–CV–1649–PSG, 2012 WL 3763794, at *1 (N.D. Cal. Aug. 29, 2012) ("Seven years after the Federal Circuit's

seminal *Phillips* decision, the cannons of claim construction are now well-known even if not perfectly understood by parties and courts alike.") Where specific claim construction doctrines are applicable, they are set forth in the body of the discussion below.

II. JUDGE WARE CORRECTLY CONSTRUED THE "SUPPLY THE MULTIPLE SEQUENTIAL INSTRUCTIONS …" PHRASE.

A. Overview.

The phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" is found in claim 1 of the '749 patent. *See* Otteson Decl., Exh. B ('749 Re-exam Cert.), 1:36 – 1:40. Plaintiffs' proposed construction differs from TPL's in that Plaintiffs improperly seek to add extraneous narrowing limitations to otherwise agreed-upon language. The competing constructions are provided below, with Plaintiffs' proposed narrowing limitations appearing in bold font.

Plaintiffs' Proposed Construction	TPL's Proposed Construction
provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide buffer that supplies one instruction at a time**	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The phrase under construction is straightforward based on its plain language: **"supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle."** To put the phrase in context, once the multiple sequential instructions have been fetched, the instructions are supplied to the central processing unit, where both the fetch and supply occur during a single memory cycle. The fact that the parties agree on the use of the words "in parallel" follows from a companion limitation that provides that the multiple sequential instructions are "fetched" in parallel. In fact, Plaintiffs and Defendants agree on much of the construction for the limitation, agreeing the phrase should be construed to mean, at least:

> provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle.

Plaintiffs, however, improperly seek to narrow the claim by importing extraneous limitations into the plain language, particularly with respect to the phrase "**without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time.**" Neither the claim nor the specification supports Plaintiffs' attempt to exclude prefetch or one-instruction-wide buffers. Importantly, the specification does not exclude systems with prefetch buffers or one-instruction-wide buffers, and none of the evidence cited by Plaintiffs' suggests otherwise. Rather, the patent teaches preferred embodiments with the ability to fetch and supply multiple instructions in parallel in a single memory cycle.

One embodiment for fetching and supplying multiple instructions in parallel to the instruction register portion of the central processing unit, during a single memory cycle, is clearly illustrated by FIGS. 2 and 4 of the '749 patent (reproduced below).

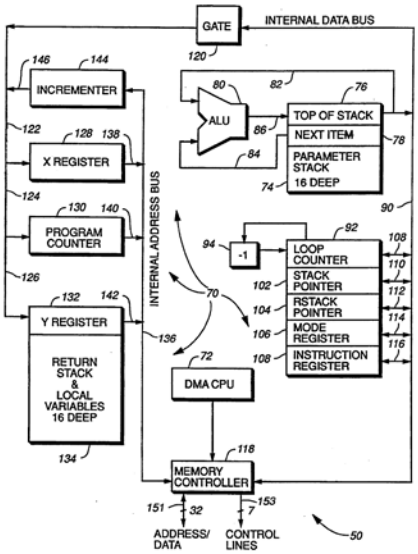

FIG._2

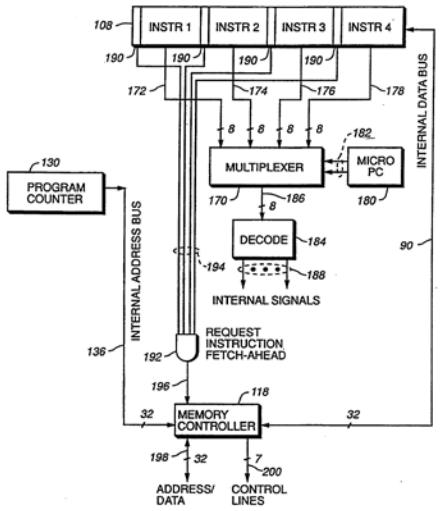

FIG._4

FIG. 2 illustrates an instruction register (108) is included within a central processing unit (70). Instructions are provided by a memory controller (118) to the instruction register (108) along an internal data bus (90). FIG. 4 illustrates in greater detail the internal data bus (which is 32-bits wide) supplying, in parallel, multiple instructions (in this embodiment, four instructions, each 8 bits wide) to the instruction register 108 during a single memory cycle.

During reexamination, the patent owner overcame a rejection under Section 102 based on the Transputer references: Edwards and May. While the Transputer references disclose fetching instructions into a prefetch buffer, the instructions are not supplied to the instruction register until a second memory cycle. As the patent owner described during reexamination, "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'" Chen Decl., Ex. 2 (1/19/10 Amendment), at 26. While the Transputer references disclose a memory controller that fetches multiple instructions, it supplies them only one at a time to a single-instruction-wide instruction buffer from which each instruction is decoded. The prior art, therefore, does not disclose supplying multiple instructions to an instruction register during the same memory cycle in which they were fetched. *See, e.g.*, the illustration of multiple instruction fetch and supply in connection with Figure 4, above.

Plaintiffs rely on four statements made by the patentee during re-examination of the '749 patent. *See* Plaintiffs Mtn. at 4-5. None of these statements is a clear disavowal of either a *prefetch buffer* ***or*** a *one-instruction-wide instruction buffer*. The only statement that even mentions "prefetch buffer" makes clear that TPL was distinguishing the supplying of instructions to the CPU one at a time and *not* the use of a prefetch buffer. In distinguishing the Edwards reference, TPL argued "[f]etching multiple instructions into a prefetch buffer ***and then supplying them one at a time is not sufficient to meet the claim limitation*** – the supplying of 'multiple sequential instructions to a CPU ***during a single memory cycle***.'" Chen Decl., Ex. 2 (1/19/10 Amendment), at 26 (emphasis added). Nothing in this statement restricts the use of a prefetch buffer, generally, as long as the device "provide[s] multiple sequential instructions in parallel to said central processing unit *in a single memory cycle*."

The remaining three statements from the '749 patent reexamination cited by Plaintiffs each similarly fail to support the restrictions Plaintiffs seek to impose. None of these statements mentions a "prefetch buffer" or a "one-instruction-wide buffer." Moreover, each statement expressly distinguishes the prior art reference on the same basis: (a) "the instructions are supplied to the CPU one at a time," (b) "although two instructions might be fetched at the same

time, one instruction is supplied to the CPU at a time," and (c) "the 'during a single memory cycle' limitation is not satisfied by supplying only one instruction to the CPU at a time." *See* Plaintiffs' Mtn., at 5 (quoting '749 reexam prosecution history). Thus, there are no clear and unmistakable disavowals of a prefetch buffer or a one instruction-wide buffer. Therefore, the portion of the construction agreed upon by the parties should be adopted.

It is important for the Court to understand the context of the reexamination statements made in connection with prefetch buffers and one-instruction-wide instruction buffers. The statements were made prior to the patent owner amending the claim to add the final "wherein" clause that defines the claim term under construction. In the end, the patent owner amended the claim to define the phrase now being construed. According to the amended claim, that "supplying" to the CPU means supplying the multiple instructions "in parallel" to the "instruction register" during the "same" memory cycle they are fetched.

B. Amended Claim 1 Supports TPL's Proposed Construction.

The clear language of the claim 1, as set out in the amendments to the claim made during reexamination, is consistent with the arguments the patent owner made in traversing the prior art and wholly support TPL's construction. The amended claim makes clear that the claimed means to fetch multiple sequential instructions from memory in parallel and supply them during a single memory cycle merely requires "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched." Otteson Decl., Exh. B ('749 Re-exam Cert.), at 1:66-2:2.

Claim 1 was amended to include a "wherein" clause which provides clear indication as to the meaning of the phrase at issue here. The wherein clause recites the following:

> *wherein*
> *the microprocessor system comprises an* ***instruction register*** *configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and wherein*
> *the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and* ***supply the multiple sequential instructions to the central processing unit*** *integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.*

Id., 1:56 – 2:2 (italics in original; underlining and bold font added).

The amendment makes clear the claimed means to fetch multiple sequential instructions from memory in parallel and supply them during a single memory cycle merely requires "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched." Otteson Decl., Exh. C (1/25/2011 Amendment) at 2 (emphasis added).

As demonstrated by his statement of reasons for patentability, the examiner agreed that the amendment clarifies the meaning of the claim language now being construed. Specifically, the examiner observed:

> Regarding **claim 1**, in the examiner's opinion, it would not have obvious to one of ordinary skill in the art to have the systems as claimed further include the features of "supplying the multiple instructions in parallel to said instruction register during the same memory cycle the multiple instructions [are] fetched." This limitation is seen to clarify the function of the current invention, which is not expressly described in the closest cited prior art of the T414 Data Sheet, the May '948 reference, MacGregor, or Koopman. Thus, the claim as presented in the amendment dated 1/25/2010, is rendered as patentable.

Otteson Decl., Exh. C (Notice of Intent to Issue a Reexam Certificate) at 8 (bold text in original). The amendment referred to in the examiner's statement is the "wherein" clause discussed above. In allowing the claim as amended, the examiner also makes clear the amendment served to "clarify" the current invention, as opposed to narrowing the unamended claim 1. *Id.* (emphasis added). The examiner's earlier allowance of reexamination claim 62, which recites a similar wherein clause, further demonstrates the examiner's understanding that the amendment clarifies the current invention, as opposed to narrowing the claim scope. *Id.*, at 10-11 ("This limitation is seen to clarify the function of the current invention ….").

In allowing the claim as amended, the PTO did not require any limiting language related to prefetch or one-instruction-wide buffers. Plaintiffs' attempt to improperly narrow the claim in that way now should be rejected. As Judge Ware found, no construction is necessary; the language is clear as it appears in the claim.

C. Plaintiffs Mischaracterize TPL's Infringement Contentions.

Plaintiffs' argument concerning TPL's infringement contentions is improper and should be rejected as a basis for claim construction. Indeed, the argument Plaintiffs' make was already rejected as premature by order of Judge Ware who found the motion improper prior to completion of claim construction. *See* Ware Order [Dkt. 361].

In any case, Plaintiffs are wrong that TPL's infringement contentions seek to recapture disclaimed subject matter. *See* Plaintiffs' Mtn., at 6-8. In its infringement contentions, TPL asserts the accused products include an instruction register as part of the CPU which is located directly upstream of a unit for decompressing 16-bit Thumb instructions. *See* Chen Decl., Ex. 4 at 7 (the blue boxes indicating the presence of an instruction register). As TPL asserts, the instruction register receives in parallel two (multiple) 16-bit Thumb instructions on a 32-bit bus upstream of the decompression and decode operations. The structure indicated by the infringement contentions, therefore, is entirely consistent with TPL's proposed construction of the phrase at issue and does not recapture subject matter purportedly disclaimed during reexamination of the '749 patent. Plaintiffs suggestion otherwise should be rejected.

III. JUDGE WARE CORRECTLY CONSTRUED THE "CLOCKING SAID CENTRAL PROCESSING UNIT" PHRASE.

A. Overview.

The phrase "clocking said central processing unit" is found in each claim of the '336 patent. Plaintiffs' proposed construction differs from TPL's in that Plaintiffs improperly seek to add extraneous narrowing limitations to otherwise agreed-upon language. The competing constructions are provided below, with Plaintiffs' proposed narrowing limitations appearing in bold font.

Plaintiffs' Proposed Construction	TPL's Proposed Construction
timing the operation of the CPU **such that it will always execute at the maximum frequency possible, but never too fast**	timing the operation of the CPU

Plaintiffs improperly seek to narrow the claim by importing extraneous limitations into the claim language, particularly with respect to the phrase "**such that it will always execute at the maximum frequency possible, but never too fast**." Plaintiffs' attempt to include this limitation violates the prohibition of reading limitations from preferred embodiments into the claims. Plaintiffs' proposed language also creates ambiguity and confusion for the jury in determining the whether the "maximum frequency possible, but never too fast" limitation is satisfied by an accused product.

B. Prior Constructions Comport with TPL's Proposed Construction.

Consistent with Judge Ware's construction of the same claim phrase and Judge Ward's construction (in the Texas action) of a related phrase, the Court here should adopt TPL's proposed construction. The phrase "clocking said central processing unit" appears in claims 1, 6 and 10 of the '336 patent. Claim 1, reproduced below, illustrates use of the term:

> 1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for **clocking said central processing unit**, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

See Otteson Decl., Exh. A ('336 Re-exam Cert.), 1:59 – 2:11 (bold text added; italics in original). As indicated by the claim, a variable speed system clock in the form of an entire ring oscillator is connected to a central processing unit. The claimed purpose of the system clock is straightforward: to clock the central processing unit. There is no requirement in the claim that the speed or frequency of the clock operate at a maximum, minimum or any other possible speed. The plain and ordinary meaning of the phrase means simply to clock or time the central processing unit, nothing more and nothing less.

The foregoing observations are consistent with Judge Ware's construction of the phrase and related constructions by Judge Ward in the Texas litigation. Judge Ware, for example, found the plain and ordinary meaning of the phrase to mean: "provide a clock signal to the central processing unit." FCCO [Dkt. 336] at 17. Finding no clear intent to limit the claim scope "using 'words or expressions of manifest exclusion or restriction,'" Judge Ware rejected the argument here again being raised by Plaintiffs and adopted TPL's proposed construction: "providing a timing signal to said central processing unit." *Id*., at 17-18 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004)).

In similar fashion, Judge Ward in the Texas litigation addressed the larger phrase in which the phrase currently under construction appears: "an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for **clocking said central processing unit**." Otteson Decl., Exh. D (6/15/2007 Ward Claim Construction Order) at 13 (emphasis added). In construing the larger phrase "oscillator … clocking," Judge Ward agreed with TPL's proposed construction that "the oscillator generates the signal(s) used for timing the operation of the CPU" and rejected an attempt by defendants to construe the oscillator as "itself determining the frequency of the signal(s) used for timing." *Id.* In other words, Judge Ward rejected an attempt by the Texas defendants to link the oscillator frequency with some undefined self-determined (or maximum) frequency, just as Plaintiffs in the current action attempt to do.

Finally, it is noted the parties to the instant action have agreed to Judge Ward's construction of the phrase "oscillator … clocking." *See* Acer Dkt. 305, Exh. A (Agreed Construction No. 19). TPL's proposed construction for "clocking said central processing unit" matches precisely the latter half of Judge Ward's construction for the larger claim phrase described above and, thus, is also consistent with the meaning of the larger phrase ascribed to and agreed upon by the parties. TPL's proposed construction is, therefore, consistent with both Judge Ware's and Judge Ward's constructions, and is also consistent with the parties agreed-upon definition of the larger phrase in which the phrase "clocking said central processing unit" appears.

C. The Court Should Reject Plaintiffs' Revised Attempt To Read Extraneous Limitations Into the Straightforward Meaning of the Phrase.

Plaintiffs urge appending an additional limitation – "such that it will execute at the maximum frequency possible but never too fast" – to the otherwise plain and ordinary meaning of "clocking said central processing unit." This additional language is excerpted from the '336 patent (*see* Otteson Decl., Exh. A, 16:59-17:2), wherein the patentee is generally describing one advantage of a preferred embodiment. In attempting to add the extraneous limitation, Plaintiffs are once again seeking to narrow a construction from Judge Ward, even though the Texas Court already considered – and rejected – the exact same argument. *See* Otteson Decl., Exh. D (6/15/2007 Ward Claim Construction Order) at 13-15 (rejecting Texas defendants' arguments relying on the same specification cites and prosecution history that Plaintiffs rely on here to argue that the CPU's processing frequency must operate at the "fastest safe operating speed"). Plaintiffs wrongly suggest that their construction is required because the patent only discloses a single embodiment. The specification of the patents-in-suit discloses multiple embodiments of the various inventions; so many that the PTO required the applicants to divide the original application into 10 separate applications.

Even in cases where a single embodiment is disclosed, importation of limitations from the specification into the claims is improper. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction."); *see also Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301 (Fed. Cir. 2003) ("The statements from the description of the preferred embodiment are simply that – descriptions of a preferred embodiment ... [which] do not indicate that the invention can only be used in such a manner."). Nowhere, however, does the patentee or patent owner ever make such a clear intention to limit the claim scope of the '336 patent.

For example, in each of the remarks made to the patent office during prosecution, the applicant carefully noted that the distinguishing feature of the '336 patent claims and the prior art was locating the clock and the central processing unit on the same integrated circuit. Chen Decl.,

Exh. 7 (Amendment, 4/15/96) at 6 ("In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit."). Placing both components on the same integrated circuit "allows" the central processing unit to track variations in the speed of the clock. *Id*. ("This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit."); Chen Decl., Exh. 7 (Amendment, 1/13/97) at 4 ("This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage."). Notably absent in each of these passages, as well as the passages cited by Plaintiffs, is language that requires the clock operate at the fastest possible speed; rather, the embodiment discussed merely allows the clock to operate at a fastest possible speed. In other words, the cited passages are merely descriptions of a preferred embodiment, that in no way "demonstrate[] a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." *Innova/Pure*, 381 F.3d at 1117. Plaintiffs' argument to the contrary should be rejected.

Further, Plaintiffs distort the prosecution history to suggest that applicants distinguished U.S. Pat. No. 4,670,837 ("Sheets") by relying upon a "feature" of the invention that the "CPU 70 executes at the fastest speed possible." *See* Plaintiffs' Mtn. at 10-11. In fact, applicants distinguished Sheets because it did not disclose an ***on-chip*** oscillator; but, rather, required a "command input control signal" to vary the frequency. Chen Decl., Exh. 7 (Amendment, 1/13/97) at 7 ("the present invention is directed to a system and method for clocking a central processing unit disposed within the same integrated circuit …"). The applicant then amended the relevant claims to "explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit." *Id.*, at 8. Thus, the basis for distinguishing Sheets was the presence of an on-chip oscillator, not the frequency of the CPU.

D. Plaintiffs' Proposed Construction is Hopelessly Vague.

Finally, Plaintiffs' proposed construction – "it will always execute at the maximum frequency possible, but never too fast" – is impermissibly vague and ambiguous, providing no guidance whatsoever on how to determine infringement or validity. For example, there is no criteria specified that would enable a jury to determine the "maximum frequency possible" or whether the CPU is going "too fast." Plaintiffs' proposed construction thus hinders, rather than helps, the trier of fact and must be rejected for that reason alone, as well as for those provided above. *See, e.g., Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1378 (Fed. Cir. 2005) (rejecting proposed construction calling for "very low dust" as ambiguous and indefinite).

For the foregoing reasons, the Court should reject Plaintiffs' attempt to improperly narrow the claimed phrase "clocking said central processing unit" and adopt TPL's straightforward construction, consistent with both Judge Ware's and Judge Ward's constructions.

Conclusion

For the foregoing reasons, Defendants respectfully request the Court enter an order adopting TPL's proposed claims constructions, consistent with Judge Ware's First Claim Construction Order.

Dated: November 2, 2012

Respectfully submitted,

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